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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,850	09/22/2003	Yossi Reuven	P-5691-US	4322
49444 7590 02/02/2007 PEARL COHEN ZEDEK LATZER, LLP 1500 BROADWAY, 12TH FLOOR NEW YORK, NY 10036			EXAMINER TORRES, JUAN A	
			ART UNIT	PAPER NUMBER
			2611	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		02/02/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/664,850

Applicant(s)

REUVEN, YOSSEI

Examiner

Juan A. Torres

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 September 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>09/22/2003</u> | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Drawings*

The drawings are objected to because:

a) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "120" and "200" have both been used to designate a mobile station; reference characters "130" and "300" have both been used to designate dual output synthesizer; reference characters "140" and "250" have both been used to transceiver; reference characters "150" and "260" have both been used to designate a first antenna; reference characters "160" and "270" have both been used to designate a second antenna.

b) The recitation in block 140 "TRANSCIEVER" is improper; it is suggested to be changed to "TRANCEIVER".

c) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "225" and "235".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Specification***

The disclosure is objected to because of the following informalities: the recitation in page 7 at the end of paragraph [0018] ""PLL 340" is improper (see figure 2); it is suggested to be changed to "PLL 330".

Appropriate correction is required.

### ***Claim Warning***

Applicant is advised that should claim 6 be found allowable, claim 17 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2611

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Brown (US 6333678 B1).

As per claim 1, Brown discloses a first phase locked loop to set a frequency of a first output signal of a first voltage controlled oscillator (figure 5 blocks 212, 102, 104, 206, 208, and 210 column 7 lines 17-26); and a second phase locked loop to receive the output signal of the first voltage controlled oscillator and to control a second voltage controlled oscillator to provide a second output signal having a frequency derived from the frequency of the first output signal (figure 5 block 516 column 7 lines 17-26).

As per claim 2, Brown discloses claim 1, Brown also discloses that the frequency of the second output signal is a rational fraction of the frequency of the first output signal (figure 5 block 516 column 7 lines 17-26 and 41-58).

As per claim 3, Brown discloses claim 1, Brown also discloses that the frequency of the second output signal is substantially similar to the frequency of the first output signal (figure 5 block 516 column 4 lines 23-50 and column 7 lines 17-26 and 41-58).

As per claim 4, Brown discloses claim 2, Brown also discloses a first synthesizer which includes the first phase locked loop and the first voltage controlled oscillator (figure 5 blocks 212, 102, 104, 206, 208, and 210 column 7 lines 17-26); and a second synthesizer which includes the second phase locked loop and the second voltage controlled oscillator (figure 5 block 516 column 7 lines 17-26).

As per claim 5, Brown discloses claim 4, Brown also discloses that the first synthesizer comprises a fractional-N synthesizer and the second synthesizer comprises an integer division synthesizer (figure 5 block 516 column 4 lines 23-50; column 6 lines 8-50 and column 7 lines 17-26 and 41-58).

As per claims 6 and 17, Brown discloses claim 4, Brown also discloses an oscillator to provide a fundamental frequency to the first synthesizer (figure 5 reference clock).

As per claim 7, Brown discloses claim 6, Brown also discloses that the oscillator includes a crystal oscillator (column 2 lines 22-30; and column 3 lines 51-66).

As per claim 8, Brown discloses generating by a first synthesizer an output signal having a frequency derived from an input signal having a desired frequency generated by a second synthesizer (figure 5 column 7 lines 17-26).

As per claim 9, Brown discloses claim 8, Brown also discloses generating the output signal comprises generating an output signal having a frequency which is a rational fraction of the desired frequency (figure 5 block 516 column 4 lines 23-50 and column 7 lines 17-26 and 41-58).

As per claim 10, Brown discloses claim 8, Brown also discloses generating the input signal using a fractional-N synthesizer (figure 5 block 516 column 4 lines 23-50 and column 7 lines 17-26 and 41-58); and generating the output signal using an integer division synthesizer (figure 5 block 516 column 4 lines 23-50 and column 7 lines 17-26 and 41-58).

As per claim 11, Brown discloses claim 8, Brown also discloses generating the input signal and the output signal from a signal having a fundamental frequency (figure 5 reference clock).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 6333678 B1) in view of Kawano (US 6181923 B1), and further in view of McLean (US 6657601 B2).

As per claim 12, Brown discloses a first phase locked loop to set a frequency of a first output signal of a first voltage controlled oscillator; a second phase locked loop to receive the output signal of the first voltage controlled oscillator and to control a second voltage controlled oscillator to provide a second output signal having a frequency derived from the frequency the first output signal. Brown doesn't disclose a transceiver operably coupled to the first and second voltage controlled oscillators and able to transmit and receive signals by at least two dipole antennas. Kawano discloses a transceiver operably coupled to the first and second voltage controlled oscillators and able to transmit and receive signals by at least two antennas (figure 1, column 7 lines 32-38). Brown and Kawano are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention, it would have been

obvious to a person of ordinary skill in the art to incorporate in the phase locked loops disclosed by Brown the transceiver disclosed by Kawano. The suggestion/motivation for doing so would have been to filter phase noise in a portable telephone terminal (Kawano column 7 lines 32-38). Brown and Kawano don't disclose that the antennas are dipole antenna. McLean discloses the use of two dipole antennas. Kawano and McLean are analogous art because they are from the same field of endeavor of wireless communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Kawano the dipole antenna disclosed by McLean. The suggestion/motivation for doing so would have been to reduce the cost of the system (McLean abstract).

As per claim 13, Brown, Kawano and McLean disclose claim 12, Brown also discloses that the frequency of the second output signal is a rational fraction of the frequency of the first output signal (figure 5 block 516 column 7 lines 17-26 and 41-58).

As per claim 14, Brown, Kawano and McLean disclose claim 12, Brown also discloses that the frequency of the second output signal is substantially similar to the frequency of the first output signal (figure 5 block 516 column 4 lines 23-50 and column 7 lines 17-26 and 41-58).

As per claim 15, Brown, Kawano and McLean disclose claim 12, Brown also discloses a first synthesizer which includes the first phase locked loop and the first voltage controlled oscillator (figure 5 blocks 212, 102, 104, 206, 208, and 210 column 7 lines 17-26); and a second synthesizer which includes the second phase locked loop and the second voltage controlled oscillator (figure 5 block 516 column 7 lines 17-26).



As per claim 16, Brown, Kawano and McLean disclose claim 15, Brown also discloses that the first synthesizer comprises a fractional-N synthesizer and the second synthesizer comprises an integer division synthesizer (figure 5 block 516 column 4 lines 23-50; column 6 lines 8-50 and column 7 lines 17-26 and 41-58).

Claims 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (US 6333678 B1) in view of Kawano (US 6181923 B1) (with Plotnik (US 6873608 B1) figure 1 for inherency of a portable telephone terminal using an internal antenna, also published as WO99/08456).

As per claim 18, Brown discloses a first phase locked loop to set a frequency of a first output signal of a first voltage controlled oscillator; a second phase locked loop to receive the output signal of the first voltage controlled oscillator and to control a second voltage controlled oscillator to provide a second output signal having a frequency derived from the frequency the first output signal. Brown doesn't disclose a mobile station having a dual output synthesizer, which includes a transceiver operably coupled to the first and second voltage controlled oscillators and able to transmit and receive signals by at least two antennas. Kawano discloses a mobile station having a dual output synthesizer, which includes a transceiver operably coupled to the first and second voltage controlled oscillators and able to transmit and receive signals by at least two antennas (figure 1, column 7 lines 32-38). Brown and Kawano are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the phase locked loops disclosed by Brown the transceiver disclosed by

Kawano. The suggestion/motivation for doing so would have been to filter phase noise in a portable telephone terminal (Kawano column 7 lines 32-38).

As per claim 19, Brown and Kawano disclose claim 18, Brown also discloses that the frequency of the second output signal is a rational fraction of the frequency of the first output signal (figure 5 block 516 column 7 lines 17-26 and 41-58).

As per claim 20, Brown and Kawano disclose claim 18, Brown also discloses that the frequency of the second output signal is substantially similar to the frequency of the first output signal (figure 5 block 516 column 4 lines 23-50 and column 7 lines 17-26 and 41-58).

As per claim 21, Brown and Kawano disclose claim 18, Brown also discloses a first synthesizer which includes the first phase locked loop and the first voltage controlled oscillator (figure 5 blocks 212, 102, 104, 206, 208, and 210 column 7 lines 17-26); and a second synthesizer which includes the second phase locked loop and the second voltage controlled oscillator (figure 5 block 516 column 7 lines 17-26).

As per claim 22, Brown and Kawano disclose claim 21, Brown also discloses that the first synthesizer comprises a fractional-N synthesizer and the second synthesizer comprises an integer division synthesizer (figure 5 block 516 column 4 lines 23-50; column 6 lines 8-50 and column 7 lines 17-26 and 41-58).

As per claim 23, Brown and Kawano disclose claim 18, Kawano also discloses a base station of a cellular communication system (figure 1, column 8 lines 35-62). Brown and Kawano are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention, it would have been obvious to a person

of ordinary skill in the art to incorporate in the phase locked loops disclosed by Brown the transceiver disclosed by Kawano. The suggestion/motivation for doing so would have been to filter phase noise in a portable telephone terminal (Kawano column 7 lines 32-38)

As per claim 24, Brown and Kawano disclose claim 18, Kawano also discloses that the antenna is used in a portable telephone terminal that inherently will use an internal antenna (figure 1, column 8 lines 35-49. See Plotnik (US 6873608 B1) figure 1 for inherency of a portable telephone terminal using an internal antenna). Brown and Kawano are analogous art because they are from the same field of endeavor of phase locked loops. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the phase locked loops disclosed by Brown the transceiver disclosed by Kawano. The suggestion/motivation for doing so would have been to filter phase noise in a portable telephone<sup>1</sup> terminal (Kawano column 7 lines 32-38).

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Myers (US 5038115 A) discloses phase coherence with frequency tracking of an input signal and for receiving weak signals in the presence of one or more stronger signals in communication systems. Yang (US 5317284 A) discloses a Wide band, low noise, fine step tuning, phase locked loop frequency synthesizer. Chen (US 5675620 A) discloses a high-frequency phase locked loop circuit. Opsahl (US 6008704 A) discloses a Fractional frequency synthesizer with

modulation lineariser. Ott (US 6636575 B1) discloses Cascading PLL units for achieving rapid synchronization between digital communications systems. Dean (US 6833764 B1) discloses synthesizing a frequency using Vernier dividers. Maeda (US 6914464 B2) discloses Phase locked loop circuit using fractional frequency divider. Peregrine ("AN3 - Using the PE3291 in Narrow Band/Paging Applications", 08/2003) discloses using the PE3291 in Narrow Band/Paging Applications. Peregrine ("AN4 - Using the PE3291/92 in CDMA Applications", 08/2003) discloses using the PE3291/92 in CDMA Applications. Peregrine ("AN5 - Using the PE329x Series Fractional-N PLL's", 08/2003) discloses using the PE329x Series Fractional-N PLL's. Peregrine ("AN6 - Minimizing Phase Noise, Spurs, Lock Time and IDD for CDMA Applications", 08/2003) discloses minimizing phase noise, spurs, lock time and IDD for CDMA Applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres  
01-23-2007

2/13/07  
JAMES HEN GHEBREHUSAE  
PRIMARY EXAMINER